AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application.

LISTING OF CLAIMS:

1. (Canceled).

2. (Currently Amended) A method of resolving timing violations in a network of components and interconnects for a physical design of an integrated circuit, the method comprising: [[as recited in claim 1,]]

performing a timing analysis on the network, one or more components or interconnects of the network, each having a particular amount of timing violation potential; and

performing a selective in-place optimization by identifying components or interconnects of the network that have the highest amount of timing violation potential and executing an in place optimization according to the identified components or interconnects;

wherein the step of performing a selective in-place optimization includes:

obtaining user-provided criteria, the criteria including cell delay, transition times, net cap and interconnect delays;

generating, in a set of reports, timing, transition, cap violation data, rc information and critical nets for the entire design;

scanning the generated reports;

performing logic operations to generate a selection list of selected components or nets or both with the greatest amount of timing violation potential based on the user-provided criteria and removing clock nets from the selection list; and

performing an in-place optimization with only the selected components or nets or both.

3. (Previously Amended) The method of claim 2, wherein the selected components or nets with greatest amount of timing violation potential are stored in a Net File.

4. (Currently Amended) The method of claim [[1]]2, wherein the selective in-place

optimization process includes at least one of: optimizing fanout, down sizing the components, and up sizing the components.

5. (Canceled).

6. (Currently Amended) A computer program embodied on computer readable medium for resolving timing violations in a network of components and interconnects for a physical design of an integrated circuit, the computer program comprising: [[as recited in claim 5,]]

code for performing a timing analysis on the network, one or more components or interconnects of the network each having a particular amount of timing violation potential; and

code for performing a selective in-place optimization by identifying components or interconnects of the network that have the highest amount of timing violation potential and executing an in place optimization according to the identified components or interconnects;

wherein the step of performing a selective in-place optimization includes:

code for obtaining user-provided criteria, the criteria including cell delay, transition times, net cap and interconnect delays;

code for generating, in a set of reports, timing, transition, cap violation data, rc information and critical nets for the entire design;

code for scanning the generated reports;

code for performing logic operations to generate a selection list of selected components or nets or both with the greatest amount of timing violation potential based on the user-provided criteria and removing clock nets from the selection list; and

code for performing an in-place optimization with only the selected components or nets or both.

7. (Canceled).